Monolithic Transistors SPST Switch for L-Band

Jorge Alves Torres, *Student Member, IEEE*, and J. Costa Freire, *Senior Member, IEEE*

***Abstract*—A comparison of single-pole single-throw switch topologies is presented in this paper. A three-MESFET monolithic GaAs switch was designed, for 2-GHz operation, fabricated and tested in three different bias conditions: $V_{\text{bias}} = 0$ (self-bias); $I_{\text{bias}} = 0$ (floating); and $V_{\text{bias}} \neq 0$, $I_{\text{bias}} \neq 0$ (biased). It will be shown that a floating configuration presents on-state lower insertion loss (IL) (∼1.7 dB). However, the off-state isolation has the same order of magnitude in all three bias conditions (typically 50 dB). Comparing measurements and simulations, the best available nonlinear model for the floating bias operation was selected. Finally, several resonant topologies were studied and a new topology is proposed to increase the off-state isolation without degrading the on-state IL. The advantages and drawbacks of resonant topologies over nonresonant configurations are also discussed, taking into account technology constraints and operation frequency. A solution to reduce the inductor value is proposed.**

***Index Terms*—MMIC, SPST, switch.**

I. Introduction

The switch is a key component for RF transceiver front-ends when the transmitter/receiver (T/R) switch is used. In personal communication systems (PCSs), the reduction of size and weight is one of the most important factors. One RF possible technology to integrate monolithically the transceiver front-end is the GaAs technology. FET switches present good isolation characteristics. Typical topologies use series and shunt FETs, with a T or π configuration, if three active devices are used. These conventional topologies have a tradeoff between isolation and insertion loss (IL): larger FET's present lower IL, but their off-state isolation degrades due to the FETs' capacitances [1]. Isolation can be increased, resonating the source and drain capacitance in the off state, with an inductance in parallel [2], [3]. However, for low frequency, such as L-band, currently widely used for PCSs, the value of such inductance is too high for monolithic integration. Another type of solution to increase the isolation is presented in [1] using an *RC* network, or in [4], where transmission lines and stubs are used to make a tank resonant shunt filter. This last solution is also not efficient in low-frequency applications.

Another T/R switch with *LC* resonators is introduced in [5] for high power at 1.9 GHz, using only a single control voltage for a single-pole double-throw (SPDT) switch. In this paper, a monolithic-microwave integrated-circuit (MMIC) single-pole single-throw (SPST) switch with MESFET technology to be used to link the antenna to the transmitter [6] and to the receiver [7] MMICs of a 2-GHz PCS transceiver is presented. Experimental and simulated results, including noise measurements, for three different bias conditions: $V_{\text{bias}} = 0$ (self-bias); $I_{\text{bias}} = 0$ (floating); and $V_{\text{bias}} \neq 0$, $I_{\text{bias}} \neq 0$ (biased) are presented. The best solution is discussed.

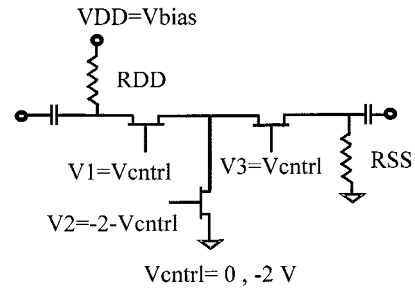

Fig. 1. MMIC SPST switch circuit.

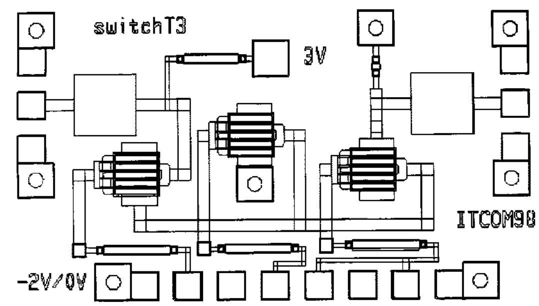

Fig. 2. MMIC layout of the SPST switch.

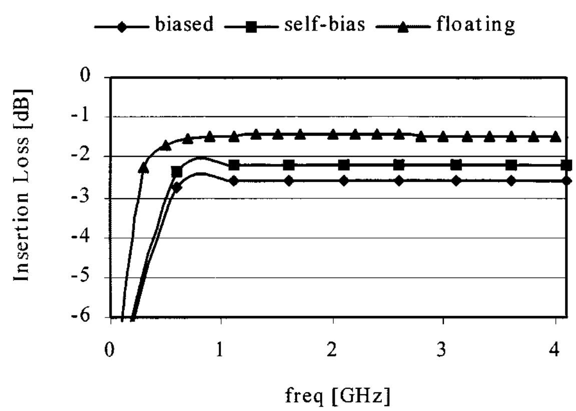

Fig. 3. Simulated on-state IL $P_{\text{in}} = -10$ dBm.

Experimental and simulation results comparison with different nonlinear MESFET models, for the best bias (floating), is presented to select the more accurate available model for each operation condition.

Using this model a study of alternative switch topologies was performed. New solutions with a good compromise iso-

Manuscript received December 29, 2000; revised May 31, 2001. This work was supported by Gabinete de gestão PRAXIS XXI under Contract PRAXIS/3/3.1/TIT/35/94.

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Publisher Item Identifier S 0018-9480(02)00764-0.

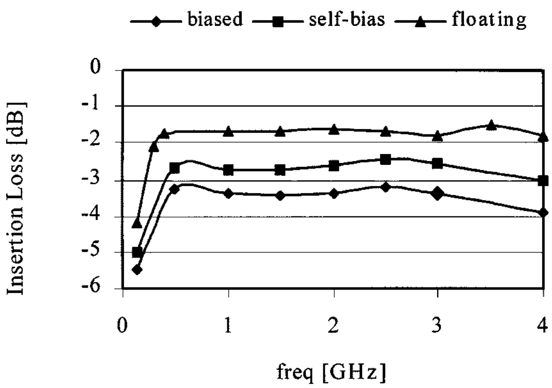

Fig. 4. Measured on-state IL $P_{\rm in} = -10$ dBm.

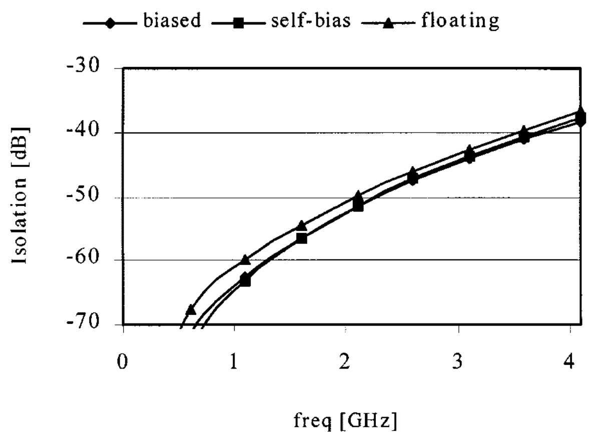

Fig. 5. Simulated off-state isolation $P_{\rm in} = -10$ dBm.

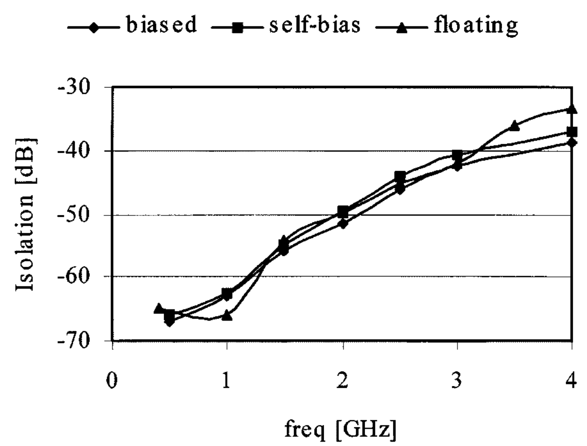

Fig. 6. Measured off-state isolation $P_{\rm in} = -10$ dBm.

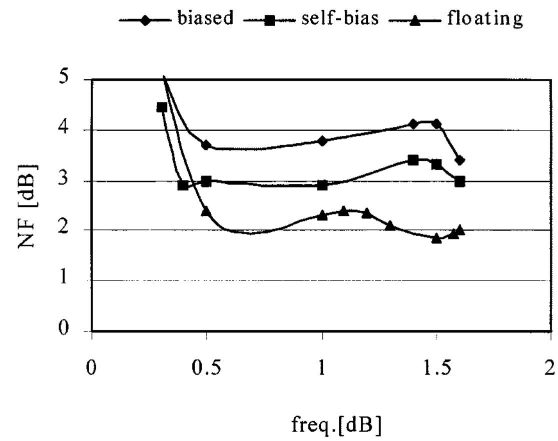

Fig. 7. Measured on-state noise figure of the SPST switch.

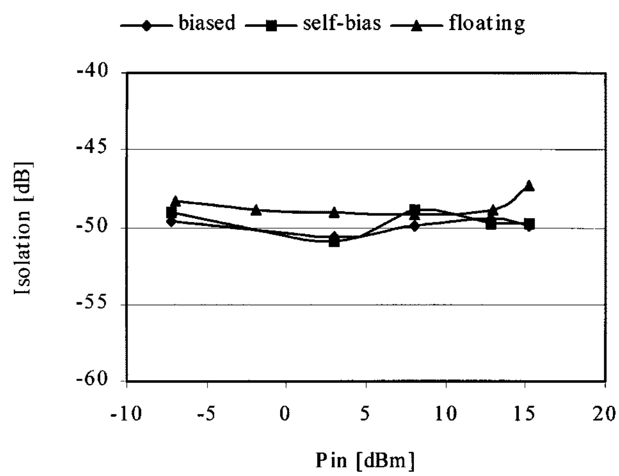

Fig. 8. Measured off-state isolation loss at 2 GHz versus input power.

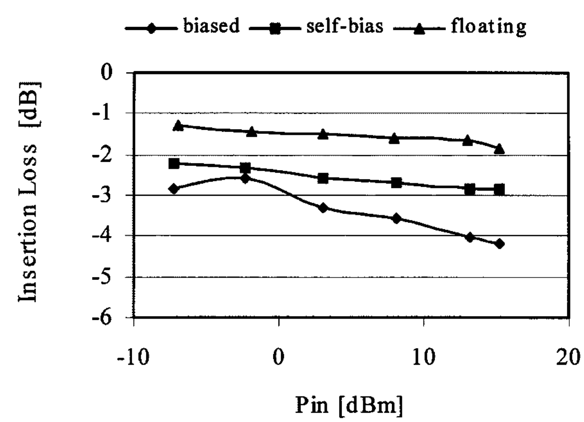

Fig. 9. Measured on-state IL at 2 GHz versus input power.

lation/loss/MMIC area are presented. For a resonant topology with an inductor between the MESFET drain and source, it is shown that it is possible to reduce the value of the inductance and, thus, the chip area, introducing a capacitor in parallel without a degradation of the on-state IL at L-band. A new resonant topology, with an *RC* T network with better performances than the single inductor, is introduced.

II. SPST MMIC Switch

An SPST MMIC switch with a T topology, consisting of three MESFETs in series–shunt–series (Fig. 1) was designed using a 0.5-μm GaAs MESFET technology [8], and its layout with an area of 1.98 mm^2 (1.07 $\times$ 1.84 mm) is presented in Fig. 2. The design main specifications are isolation higher than 50 dB with IL lower than 1.5 dB at 2 GHz. The circuit is dc decoupled. Large transistors were used (600-μm gatewidth) to allow low IL. The switch control voltages are -2 and 0 V. The bias resistors are optimized for a compromise between isolation and IL. The current bias is 1 mA in the on state with a $V_{\rm bias} = 3$ V.

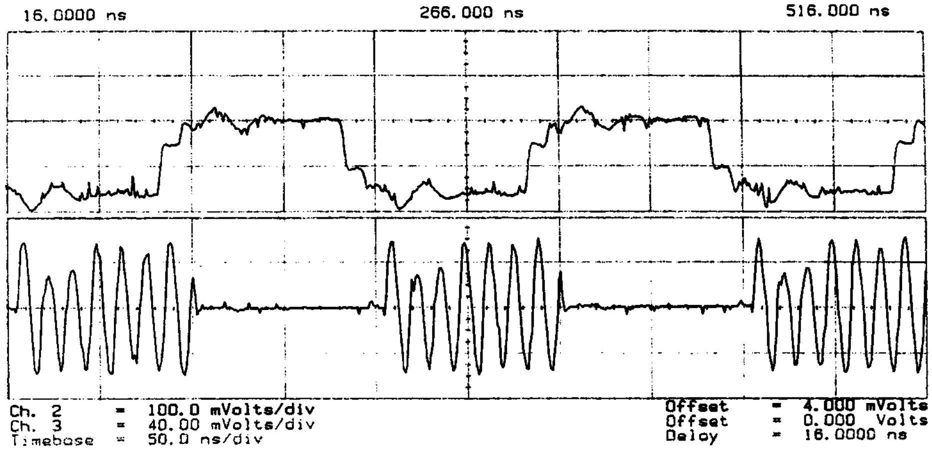

Fig. 10. Measured SPST floating switch transient behavior (ch.2 sub-sampled 1920-MHz output RF signal, ch.3 $V_2 = 0/2$ V @ 5-MHz control signal).

The prototype was tested with $P_{\rm in} = -10$ dBm and with and without the MESFET's external dc bias to verify its influence on the switch performances. Without dc bias, the following two solutions were tested: $V_{\rm bias} = 0$ V (self-bias) and $I_{\rm bias} = 0$ (floating). The floating circuit was obtained by removing the RSS source resistor that is grounded through a via (Fig. 1).

Simulations using a Curtice cubic (CC) model for the MESFET with a harmonic-balance simulator or with a linear simulator are close to the measurements results for $V_{\rm bias} = 3$ V and $V_{\rm bias} = 0$ V. The results for on-state IL are presented in Figs. 3 and 4, while off-state isolation results are presented in Figs. 5 and 6.

From 1–4 GHz, the input and output return loss are always better than -15 dB for the three bias conditions [9].

These results show that the floating switch has a better performance, mainly lower IL, and the biased switch is the worst solution.

Noise figure for the on state was also measured until 1.6 GHz (Fig. 7) and, again, better results are obtained for the floating switch and worst for $V_{\rm bias} = 3$ V, which are in agreement with the loss experimental results (Fig. 4).

Measurements for higher input power show that the performance of the SPST switch is not degraded with large signals, presenting a 1-dB compression point higher than 15 dBm (Figs. 8 and 9).

The transient behavior of the SPST floating switch was measured applying two 50% duty cycle square waves out-of-phase to $V_1 = V_3$ and V_2. The curves in Fig. 10 were obtained with a digital oscilloscope for an input continuous wave (CW) signal of 1920 MHz with -3 dBm and a control signal of 5 MHz with 0/2 V of magnitude.

The output signal was sub-sampled for a better visualization. Due to the oscilloscope characteristics, an offset of -1 V and a 30-dB attenuator were introduced in the control signal measurement channel. The output signal was simultaneously measured on a spectrum analyzer with a 3-dB coupler. The 130 mV measured predicts 1.6 dB of IL, which is in agreement with the S_{21} small-signal measurements (Fig. 4).

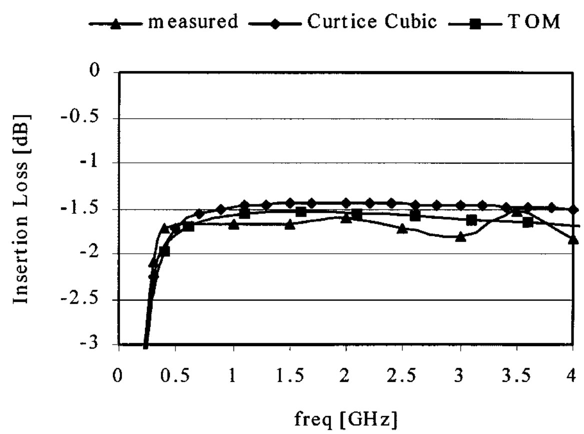

Fig. 11. Measured and simulated on-state IL $P_{\rm in} = -10$ dBm floating topology.

III. Nonlinear MESFET Models Accuracy

With a MESFET CC model, a TriQuint own model (TOM), and an EEFET3 model supplied by the foundry and a Tajima modified model obtained from continuous (CTM) or pulsed (PTM) measurements extracted by the authors, experimental and simulation results comparison for the floating switch were performed. For the on-state operation, all the models present similar results predicting better IL than measurements (Fig. 11). To not overcharge the figure, the results for EEFET3, CTM, and PTM models were not shown. The TOM model results are slightly closer to the measurements. However, the differences among the different models are not significant (less than 0.2 dB).

For the off-state operation, the more accurate model is the CC (Fig. 12). All the other models had presented results very similar to the TOM model. For the same reason mentioned above, only the TOM and CC results are depicted in Fig. 12. Accordingly, the CC model was used in the study of resonant topologies presented in Section IV. We emphasize that this choice is only valid for this application (SPST floating switch). For other applications, the choice should be different since the device has different bias.

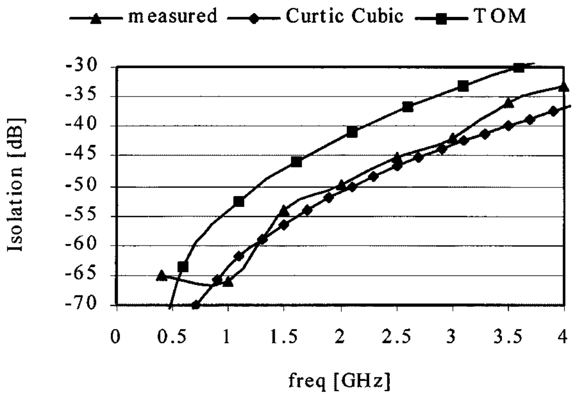

Fig. 12. Measured and simulated off-state isolation $P_{\rm in} = -10$ dBm floating topology.

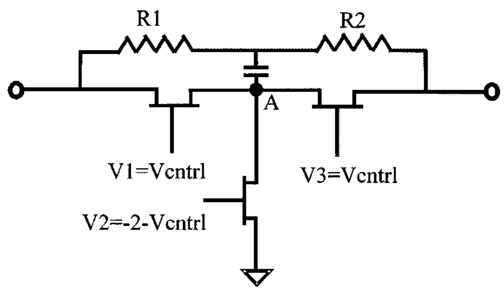

Fig. 13. Resonant *RC* switch circuit.

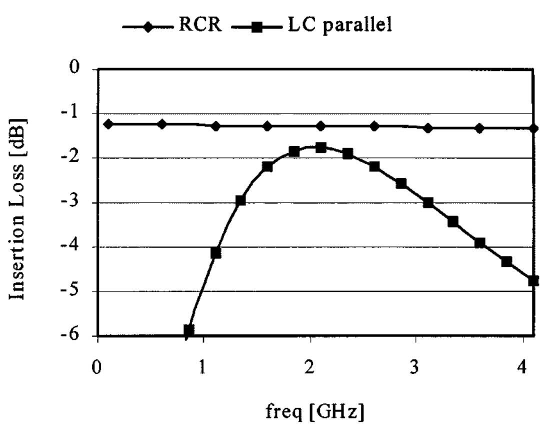

Fig. 14. Simulated on-state IL of resonant switches.

IV. Resonant Switches

In order to increase the off-state isolation using the CC model, two topologies of resonant switches were studied. The first includes an *RC* T network (Fig. 13). We have noticed that better results are obtained if we connect the capacitor to the internal node A and not to the ground, as proposed in [1]. The proposed circuit has a narrower band, but is enough for many applications (Figs. 14 and 15). The values of R and C components used to resonate the isolation at 2 GHz were $R_1 = 1.416$ KΩ, $C = 3.1$ pF, and $R_2 = 172\ \Omega$ for 600-μm transistors.

The second topology studied is presented in Fig. 16. It was observed that this topology, using an inductor connected to both drain and source, making a tank circuit with $C_{\rm ds}$, can only be implemented at higher frequencies, due to the MMIC inductors maximum values. It can be seen in Figs. 5 and 6 that the simple

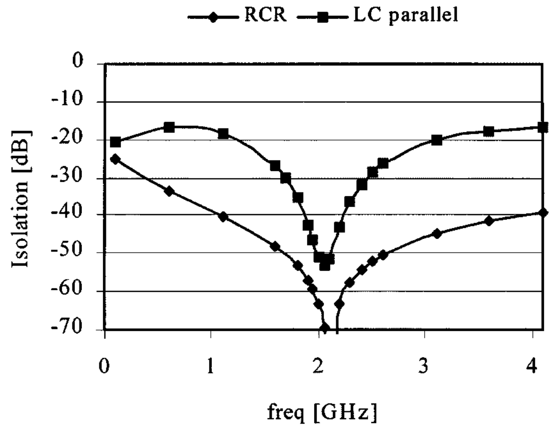

Fig. 15. Simulated off-state isolation of resonant switches.

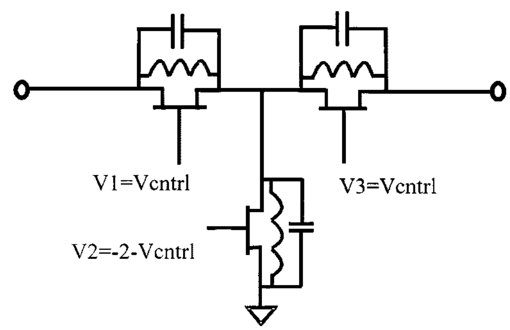

Fig. 16. Resonant *LC* switch circuit.

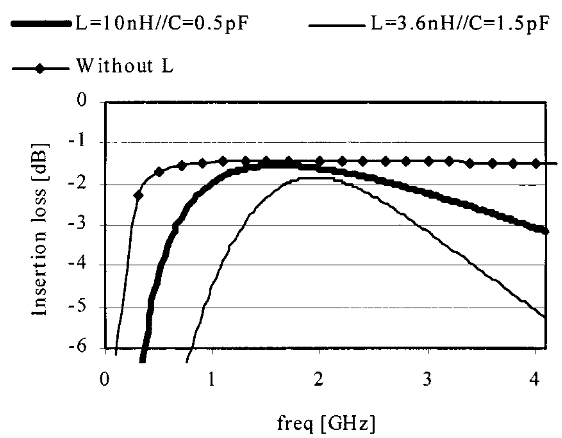

Fig. 17. Simulated on-state IL of *LC* resonant switches, compared with nonresonant switch.

SPST switch isolation is degraded with frequency. Accordingly, at low frequencies, the advantage of using a resonance is not significant. From Figs. 14 and 15, we can conclude that the *RC* resonant switch not only presents lower IL and higher isolation than the inductor resonant switch, but also presents higher bandwidth.

If an additional capacitor is used in parallel with the inductor, we can reduce the value of the inductance to a feasible value, reducing the chip area without degradation of the on-state IL (Figs. 17 and 18). For transistors with larger gatewidth W, the value of $C_{\rm ds}$ is increased and a lower inductance is needed for a given frequency. For instance, at 2 GHz, a 300-μm gatewidth

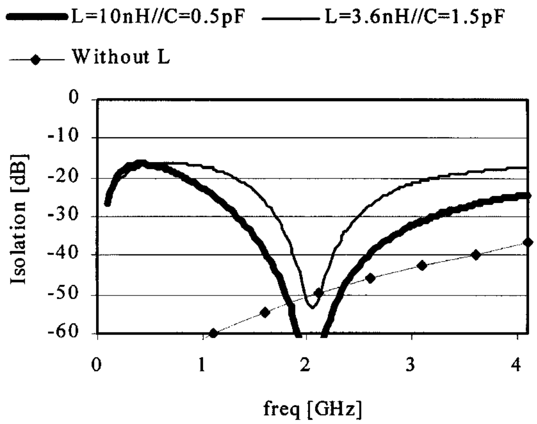

Fig. 18. Simulated off-state isolation of *LC* resonant switches, compared with nonresonant switch.

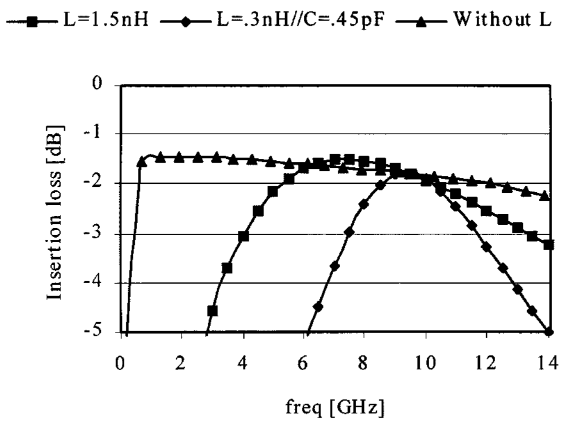

Fig. 19. Simulated on-state IL of *LC* and *L* resonant switches at 11 GHz, compared with nonresonant switch.

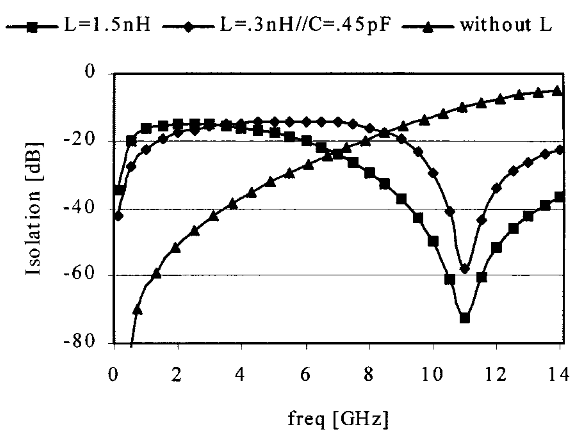

Fig. 20. Simulated off-state isolation of *LC* and *L* resonant switches at 11 GHz, compared with nonresonant switch.

MESFET needs an inductance of 86 nH and for a 600-μm MESFET, only 41 nanohenrys are needed. Using a capacitor $C = 0.5$ pF in parallel with the 600-μm gatewidth MESFET, the inductor for 2 GHz is $L = 10$ nH, and for $C = 1.5$ pF, is $L = 3.6$ nH. These last values were used in Figs. 14 and 15 simulations.

In Figs. 17 and18, it is noticed that reducing the inductor from 10 to 3.5 nH degrades the IL only 0.2 dB, but the isolation is almost the same as without resonances. However, for higher frequency, the reduction of the inductor size is effective. At 11 GHz a 5$\times$ reduction of the inductor (using the parallel capacitor) only degrades IL in 0.2 dB and isolation in 15 dB (from 72 to 57 dB), which is still better than the 10 dB obtained without resonance (Figs. 19 and 20).

Additionally, with the lower inductor, the minimum IL and the maximum isolation frequencies are closer (Figs. 19 and 20).

V. Conclusions

An SPST GaAs monolithic switch has been presented in this paper. It has been emphasized that better performance (IL of 1.7 dB and isolation of 50 dB) was obtained with a floating bias ($I_{\rm bias} = 0$).

Five MESFET nonlinear models have been used on the simulations and the most accurate to predict the floating-bias SPST switch behavior was the CC supplied by the foundry. Accordingly, this model was used to study improved resonant topologies.

A effective solution to reduce the inductor value in *LC* resonant switches for mid-frequency applications and a new topology of *RC* resonant switch for low-frequency applications have been proposed.

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